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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,777	04/17/2001	Gary D. Martin	AMCC-002XX	6860

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EXAMINER	
MEW, KEVIN D	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,777	MARTIN, GARY D.	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-8 and 10-12* is/are rejected.

7)☒ Claim(s) *5, 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Response to Amendment

1. Applicant's Remarks/Arguments filed on 2/25/2005 regarding claims 1-4, 6-8, 10-12 have been considered. Claims 1-12 are currently pending.

2. Acknowledgement is made of the amended abstract regarding the objection to the specification cited in the previous Office Action. The correction is acceptable and the objection to the specification has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-8, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Diaconescu et al. (USP 6,738,395).

Regarding claims 1, 7, 11, Diaconescu discloses a SONET multiplexed communications system (see element 10, Fig. 3 and col. 6, lines 1-10) to perform a method, comprising:

at least one SONET input signal path configured to receive at least one input signal (see SONET input path, see element 12, Fig. 3);

at least one SONET output signal path configured to transmit at least one output signal corresponding to the input signal (SONET output path coming out of data collecting block, see element 20, Fig. 3); and

a time slot interchange circuit operatively coupled between the SONET input and output signal paths (Time Slot Interchange TSI block, see element 16, Fig. 3 and col. 6, lines 10-14) and configured to provide time division multiplexed connections for the input and output signals (Time Slot Interchange TSI block operation within block 16 mirrors that of a TSI block operation of block 20, see col. 6, lines 27-41),

wherein the SONET input signal path includes a pointer interpreter configured to interpret at least one input signal pointer (a pointer processing strip comprises a pointer interpreter for interpreting an input, see col. 4, lines 43-62) serially coupled to a synchronization buffer (Elastic Store, see col. 4, lines 15-26 and Figs. 1 and 3) configured to transfer the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit (the processing strip adjusts input data in a line clock domain to output data in a system clock domain, see col. 6, lines 15-26), and

wherein the SONET output signal path (processing strip 14 in the output path) includes a pointer generator (includes a pointer generator, see col. 6, lines 15-26 and Figs. 1 and 3) configured to generate at least one output signal pointer (pointer generator serially coupled to pointer interpreter delay block in block 18, see Fig. 3) serially coupled to a first-in first-out buffer (delay block 18 is implemented as a FIFO register, see col. 7, lines 8-18) configured to transfer the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path (data input is received in a line clock

domain at the TSI block of the distribution block 16 to output data in a system clock domain, see col. 6, lines 15-26).

Regarding claim 2, Diaconescu discloses the system of claim 1 wherein the pointer interpreter SONET (pointer interpreter in processing strip 14, see Fig. 1) precedes the synchronization buffer (Elastic Store, see Fig. 1) in the SONET input signal path (pointer interpreter precedes Elastic Store in the SONET input path, see Fig. 1).

Regarding claim 3, Diaconescu discloses the system of claim 1 wherein the synchronization buffer precedes the pointer interpreter in the SONET input signal path.

Regarding claims 4, 12, Diaconescu discloses the system to perform a method, wherein the input signal STS-M (M > 1) signal (STS-12, STS-24 or STS-24 signals, see col. 6, lines 15-26), and SONET input signal path (see Fig. 3) further includes an alignment buffer (pointer interpreter delay block, see element 18, Fig. 3) operatively coupled between the synchronization buffer (Elastic Store within processing strip 14, Fig. 3) and the time slot interchange circuit (pointer interpreter delay block 18 is coupled between Elastic Store in processing strip 14 and TSI block 16 in element 16, see Fig. 3) and configured to perform column alignment on the STS-M signal (pointer interpreter delay block is configured to control input data reading on at least a pair of an ith and jth pointer processing strips such that corresponding input data is read on the jth pointer processing strip after a predetermined number pointer interpreter pair delay from a

time when corresponding input data is read on the ith pointer processing strip, see col. 3, lines 60-67 and col. 6, lines 1-14).

Regarding claims 6, 10, Diaconescu discloses the system to perform a method, wherein the at least one SONET input signal path (input path 12, Fig. 3) comprises a plurality of SONET input signal paths (a plurality of input paths going into processing strips 14, see Fig. 3) and the least one SONET output signal path (output path coming out of block 20, see Fig. 3) comprises a plurality of SONET output signal paths (a plurality of paths coming out of processing strips 14, see col. 6, lines 49-54), the number of SONET input signal paths being greater than the number of SONET output signal paths (the number of input paths going into processing strips 14 is greater than the number of output path coming out of block 20, see Fig. 3).

Regarding claim 8, Diaconescu discloses the system of claim 7 wherein the input signal STS-M (M > 1) signal (see col. 10, lines 42-47), and SONET input signal path (see Fig. 6) further includes an alignment buffer (multiplexer 411, Fig. 6) operatively coupled between the synchronization buffer (cell buffer 460) and the time slot interchange circuit (elements 424, 428, 429, 422, Fig. 6) and configured perform column alignment on the STS-M signal (each channel on the incoming lines is assigned a predetermined fixed time location with the high-speed SONET frame stricture, see col. 10, lines 42-65).

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 6-8, 10-12 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

5. Claims 5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In claims 5 and 9, the alignment buffer includes a multitap delay element and a controller circuit, the multitap delay element having an input and a plurality of outputs and being configured receive STS-M signal the input and provide increasingly delayed versions of the STS-M signal at successive ones outputs, controller circuit being configured select a delayed version of the STS-M signal from one outputs application the time interchange circuit.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with respect to time slot interchanging of time slots from multiple sonet signals without first passing the signals through pointer processors to synchronize them to a common clock.

US Patent 6,188,692 to Huscroft et al.

US Publication 2002/0080812 to Stadler et al.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER

KDM
Art Unit 2664